EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	22	("4744084"|"5095454"|"5365463" |"5608645"|"5651012"|"5826061" |"5850355"|"5867691"|"6338127" |"6408265"|"6430731").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/24 14:59
S2	0	((domain near3 cross$3) adj3 signal) and (delay near3 randomiz$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/24 15:16
S3	5	((domain near3 cross$3)) and (delay near3 randomiz$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/24 15:02
S4	30	((domain near3 cross$3)) and (delay near3 random$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/24 15:02
S5	54	((domain near3 (cross$3 or dissimilar or different))) and (delay near3 random$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/24 15:15
S6	2	"20060044026"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/24 15:15
S7	97	((domain near3 cross$3) adj3 signal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/25 11:14
S8	585	(circuit same verif$6) and (asynchronous and (flip adj2 flop) and synchroniz$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/25 11:15

EAST Search History

S9	98	(circuit same verif$6) and (asynchronous same(flip adj2 flop) same synchroniz$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:03
S10	96	S9 and cycl$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/25 11:16
S11	18	("4787062" | "5014226" | "5259006" | "5418931" | "5475830" | "5790836" | "5923193" | "6088821").PN. OR ("6353906").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/07/25 12:20
S12	1	"6353906".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/07/25 12:20
S13	113	(circuit same (verif$6 or simulat$4)) and (asynchronous same clock) and ((flip adj2 flop) same synchroniz$6) and metastab$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:04
S14	98	(circuit same verif$6) and (asynchronous same(flip adj2 flop) same synchroniz$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:04
S15	65	S13 not S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:04
S16	19	S15 and (clock or asynchronous).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:11
S17	399	(circuit same asynchronous same (verification or simulation))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:11

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S18	508	(circuit same asynchronous same (verification or simulat$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:12
S19	166	S18 and (flip adj2 flop)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:12
S20	105	S19 and clock and period	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:12
S21	101	S20 not S16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:12
S22	101	S21 not S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:32
S23	2439	(asynchronous and ((verification or simulation) or circuit)).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:37
S24	2435	S23 not S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:33
S25	222	S24 and flip-flop	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:33

S26	79	S25 and clock and period	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:33
S27	7	"6088821"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 10:37

Google Scholar

(simulation OR verification) asynchronous cloc   Search

Scholar Results 1 - 10 of about **206** for (simulation OR verification) asynchronous clock synchronizer flip

Simulation and Synthesis Techniques for Asynchronous FIFO   All articles Recent articles
Design with Asynchronous Pointer ... - group of 3 »
CE Cummings, P Alfke - Proceedings of the Synopsis User Group (SNUG) Papers and ..., 2002 - sunburst-design.com
... **Simulation** and Synthesis Techniques for **Asynchronous** ... The technique described implements
an **asynchronous** assertion of ... to analyze for static timing **verification**. ...
Cited by 8 - View as HTML - Web Search

Fourteen ways to fool your synchronizer - group of 7 »
R Ginosar - Asynchronous Circuits and Systems, 2003. Proceedings. Ninth ..., 2003 - ieeexplore.ieee.org
... A powerful protocol **verification** algorithm might provide a useful tool to ... SOC, a
global reset signal is naturally **asynchronous** to at least some of the **clock** ...
Cited by 13 - Web Search

Performance of synchronous and asynchronous schemes for VLSI systems - group of 6 »
M Afghahi, C Svensson - IEEE Transactions on Computers, 1992 - doi.ieeecs.org
... For example, **simulation** showed that a **clock** pulse ... interconnection line - - - - and
a complete **clock** path ... AND SVENSSON: SYNCHRONOUS AND **ASYNCHRONOUS** SCHEMES FOR ...
Cited by 55 - Web Search

A fast resolving BiNMOS synchronizer for parallel processor interconnect - group of 3 »
J Jex, C Dike - Solid-State Circuits, IEEE Journal of, 1995 - ieeexplore.ieee.org
... can be easily checked during silicon validation and **simulation** error correlation ...
The divided **clock**, however, requires that the **asynchronous** input stream ...
Cited by 9 - Web Search - BL Direct

Optimization of CMOS arbiter and synchronizer circuits with submicrometer MOSFETs -
group of 3 »
T Sakurai - Solid-State Circuits, IEEE Journal of, 1988 - ieeexplore.ieee.org
... A formerly reported **simulation** technique to obtain the ... f2 are frequencies of two
asynchronous clocks, that is ... arbiters, and data and latch **clock** frequencies for ...
Cited by 24 - Web Search

Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs -
group of 9 »
CE Cummings - Synopsys Users Group Conference, San Jose, CA, www. sunburst ..., 2001 - sunburst-design.com
... data, control-signal and **verification** handling to ... timing analysis, synthesis and
simulation methodologies to ... **flip-flop** samples the **asynchronous** input signal ...
Cited by 5 - View as HTML - Web Search

Formal Verification of Synchronizers - group of 5 »
T Kapschitz, R Ginosar - Lecture notes in computer science - www-ee.technion.ac.il
... describes how to generate formal **verificati** n executions of ... PSL [9]) for any
multi-**clock** domain system ... with modeling of mutually **asynchronous cl cks** in Section ...
Cited by 3 - View as HTML - Web Search

Reproducing synchronization bugs with model checking - group of 6 »